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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,980	07/17/2003	Yun Shon Low	VP085	2164

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EXAMINER	
PERVAN, MICHAEL	
ART UNIT	**PAPER NUMBER**
2677	

DATE MAILED: 12/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/621,980	LOW ET AL.	
	Examiner	Art Unit	
	Michael Pervan	2677	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-20* is/are rejected.

7)☒ Claim(s) *9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/17/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5, 7, 10-14, 16 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamamoto (US 6,043,798).

In regards to claim 1, Yamamoto discloses driving a display panel (101; first display with memory characteristics) and peripheral devices (201; second display without memory characteristics) associated with the display panel through common data lines comprising identifying a non-display period for the display panel (Figure 1, col. 5, lines 65-67 and col. 6, lines 1-7), causing a peripheral device interface (Figure 1, 500) corresponding to one of the peripheral devices (Figure 1, 201) to transmit control data over a control line associated with the peripheral device (col. 4, lines 62-67 and col. 5, lines 1-10), selecting data associated with the one of the peripheral devices for transmission through the common data lines during the non-display period (col. 5, lines 47-52 and col. 7, lines 36-46; blanking period is interpreted as the non-display period) and maintaining an image quality for an image being display on the display panel while the common data lines are being used for communicating with the one of the peripheral devices (col. 6, lines 58-64).

In regards to claim 2, Yamamoto discloses method of operation of identifying a non-display period (blanking period) for the display panel including monitoring a display panel active signal (col. 7, lines 36-46).

In regards to claim 3, Yamamoto discloses method operation of causing a peripheral device interface corresponding to one of the peripheral devices to transmit control data over a control line associated with the peripheral device includes transmitting an enable signal (interpreted to mean a signal that enables a device to perform its particular function) to the peripheral device interface (col. 6, lines 58-64 and col. 7, lines 36-46; if the Unit ID is the same then the device becomes enabled and data is transferred).

In regards to claim 4, Yamamoto discloses transmitting a select signal configured to select data originating from the peripheral device interface (col. 7, lines 36-46; when the id is different it selects the second display to monitor DHBL and send a demand for transfer on detection of DHBL becoming "L").

In regards to claim 5, Yamamoto discloses after selecting data associated with the one of the peripheral devices for transmission through the common data lines during the non-display period (blanking period), the method includes selecting the data associated with the one of the peripheral devices rather than data associated with the display panel (col. 7, lines 10-20 and 36-46).

In regards to claim 7, Yamamoto discloses a graphics controller comprising a memory region 402 configured to store image data for display on a display panel in communication with the graphics controller (Figure 4), interface circuitry modules 310

and 510 respectively, where each of the interface circuitry modules is configured to transmit data from the graphics controller over a set of shared data lines (Figures 3 and 5), selection circuitry configured to select data from one of the interface circuitry modules for transmission over the set of shared data lines and line sharing circuitry configured to inform each of the interface circuitry modules to transmit control data 404-407 (Figure 4), the line sharing circuitry further configured to generate select signals for the selection circuitry, the select signals enabling the selection circuitry to select the data from one of the interface circuitry modules 403 (Figure 4).

In regards to claim 10, Yamamoto discloses interface circuitry modules are selected from the group consisting of a display panel controller interface, a camera controller interface and an external memory interface 300 and 500 (Figure 1).

In regards to claim 11, Yamamoto discloses the line sharing circuitry being further configured to assert a display panel select signal during an active display period (col. 5, lines 65-67 and col. 6, lines 1-7; UNIT ID could be either the display panel or the peripheral device).

In regards to claim 12, Yamamoto discloses the line sharing circuitry being further configured to assert a peripheral device select signal during a non-display period (col. 5, lines 65-67 and col. 6, lines 1-7; UNIT ID could be either the display panel or the peripheral device).

In regards to claim 13, Yamamoto discloses interface circuitry modules including a peripheral device interface circuitry module (Figure 5), the peripheral device interface circuitry module configured to read data from a peripheral device wherein the data from

the peripheral device is transmitted over the set of shared data lines (col. 7, lines 10-16).

In regards to claim 14, Yamamoto discloses a device comprising central processing unit 401 (Figure 4), display panel 101 (Figure 1), peripheral component 201 (Figure 1) and graphics controller 420 in communication with the CPU (Figure 4), the graphics controller configured to drive the display panel and the peripheral component over a shared set of data lines (col. 5, lines 56-63), the graphics controller including circuitry configured to select one of display data and peripheral component data for transmission over the shared set of data lines based upon a display mode signal associated with the display panel (col. 6, lines 8-13).

In regards to claim 16, Yamamoto discloses shared set of data lines as being bi-directional (Figure 5 and col. 7, lines 10-20; the peripheral device sends a signal out on the BUSYi lines and receives data from the PDi lines which are carried over the same lines).

In regards to claim 19, Yamamoto discloses circuitry configured to select one of display data and peripheral device data for transmission over the shared set of data lines based upon a display mode signal associated with the display panel (col. 5, lines 25-46) including interface circuitry modules where each of the interface circuitry modules (Figure 1, 300 and 500) are configured to transmit data from the graphics controller over the shared set of data lines (col. 5, lines 57-64), selection circuitry configured to select data from one of the interface circuitry modules for transmission over the shared set of data lines 404-407 (Figure 4) and line sharing circuitry (Figure 4,

403) configured to inform each of the interface circuitry modules to transmit control data (col. 5, lines 65-67 and col. 6, lines 1-7)), the line sharing circuitry further configured to generate select signals for the selection circuitry, the select signals enabling the selection circuitry to select the data from one of the interface circuitry modules (col. 6, lines 8-13).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 6 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto in view of Rondel et al. (US 4,984,177).

In regards to claim 6, Yamamoto discloses method operation of maintaining an image quality for an image being displayed on the display panel while the common data lines are being used for communicating with the one of the peripheral devices, including accessing an internal memory to maintain the image quality (col. 6, lines 58-64). Yamamoto does not disclose the internal memory being random access memory.

Rondel discloses accessing an internal random access memory to maintain image quality (col. 6, lines 45-47). It would have been obvious at the time of invention to modify Yamamoto with the teachings of Rondel because random access memory (RAM) allows access to information in any order and can be written to and read from.

In regard to claim 20, Yamamoto does not disclose display panel including random access memory.

Rondel discloses display panel including random access memory (col. 6, lines 45-47). It would have been obvious at the time of invention to modify Yamamoto with the teachings of Rondel because random access memory (RAM) allows access to information in any order and can be written to and read from.

5. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto in view of Wong et al (US 5,963,192).

In regards to claim 8, Yamamoto does not disclose selection circuitry including a first multiplexer and a second multiplexer.

Wong discloses selection circuitry including a first multiplexer and a second multiplexer. It would have been obvious at the time of invention to modify Yamamoto with the teachings of Wong because it is more reliable since you are assured to receive the correct output according to the select signal sent to the multiplexer.

6. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto.

In regards to claim 15, Yamamoto discloses number of shared lines being equal to sixteen. Yamamoto does not disclose number of shared lines being equal to eighteen. Since no benefit or advantage to having eighteen shared data lines was described in the specification, the examiner believes this to be a designers choice and that sixteen shared data lines will perform the same functionality as eighteen.

7. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto in view of Kikuchi (US 2004/0183895).

In regards to claim 17, Yamamoto does not disclose the peripheral device as being one of a digital camera and an external memory.

Kikuchi discloses the peripheral component as being one of a digital camera 8 and an external memory (Figure 3). It would have been obvious to modify Yamamoto with the teachings of Kikuchi because it provides more functionality to the device and allowing the user to use one device in place of two.

8. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto in view of Taniguchi et al (US 2004/0058715).

In regards to claim 18, Yamamoto does not disclose the device to be a cellular phone having a first section including the CPU and the graphics controller and a second section including the display panel and the peripheral component, wherein the shared set of data lines enable communication between first section components and second section components.

Taniguchi discloses the device to be a cellular phone having a first section including the CPU and the graphics controller and a second section including the display panel and the peripheral component, wherein the shared set of data lines enable communication between first section components and second section components (Figures 1 and 2). It would have been obvious at the time of invention to modify Yamamoto with the teachings of Taniguchi since it would lead to a more compact and easier to carry device.

Allowable Subject Matter

9. Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Pervan whose telephone number is (571) 272-0910. The examiner can normally be reached on Monday - Friday between 8am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MVP
Dec. 7, 2005

AMR A. AWAD
PRIMARY EXAMINER